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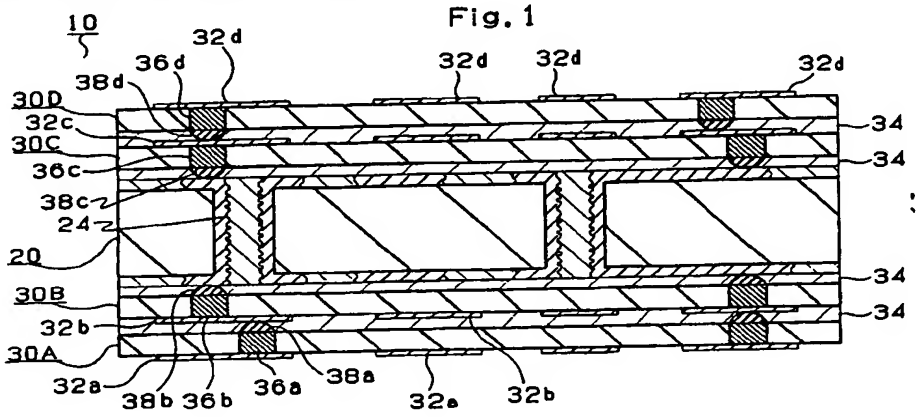
(54) MULTILAYER PRINTED WIRING BOARD AND METHOD FOR MANUFACTURING THE SAME

(57) Holes (40a) are formed with a laser beam through an insulating substrate (40) on which a metallic layer (42) if formed. After the holes (40A) are formed, via holes (36a) are formed by filling up the holes (40a) with a metal (46) and a conductor circuit (32a) is formed by etching the metallic layer (42). Then, a single-sided circuit board (30A)is formed by forming projecting conductors (38a) on the surfaces of the via holes (36a). The projecting conductors (38a) of the circuit board (30A) are put on the conductor circuit (32b) of another single-sided circuit board (30B) with adhesive layers (50) composed of an uncured resin in between and heated and pressed against the circuit (32b). The projecting conductors (38a) get in the uncured resin by pushing aside the resin and are electrically connected to the circuit (32b). Since single-sided circuit boards (30A, 30B, 30C, and 30D) can be inspected for defective parts before the boards (30A, 30B, 30C, and 30D) are laminated upon another, only defectless single-sided circuit boards can be used in the step of lamination.

Fig. 1



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Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a multilayer printed wiring board and method for manufacturing the same, and more particularly to a multilayer printed wiring board having an interstitial via hole (IVH) structure and a method for manufacturing the same.

Description of the Related Art

[0002] A conventional multilayer printed circuit board is constituted by a laminate obtained by alternately laminating copper-clad laminates and prepregs. The laminate has a surface on which a surface wiring pattern has been formed. Moreover, an internal wiring pattern is formed between interlayer insulating layers. Through holes are, by punching formed in the direction of the thickness of the laminate to establish the electric connections among internal wiring patterns or among internal wiring patterns and the surface wiring patterns.

[0003] The multilayer printed circuit board having the above-mentioned through hole structure must have regions for forming the through holes. Therefore, the density at which elements are mounted cannot be easily raised. As a result, there arises a problem in that the multilayer printed circuit board having the through hole structure cannot easily address needs for considerable reductions in the sizes of the portable electronic apparatuses, realizing narrow pitch packages and practical use of MCM.

[0004] As an alternative to the foregoing multilayer printed circuit board having the through hole structure, a multilayer printed circuit board has recently received attention which is formed into a full-thickness interstitial via-hole (IVH) structure which is able to easily address raising of the density.

[0005] The multilayer printed circuit board having the full-thickness IVH structure is a printed circuit board having a structure in which via holes for electrically connecting conductive layers to one another are formed in each of the interlayer insulating layers which constitute the laminate. That is, the foregoing printed circuit board has the via holes (buried via holes or blind via holes) which do not penetrate the substrate on which the circuit is formed and which electrically connect the internal wiring patterns to one another or the internal wiring patterns and the surface wiring patterns to one another. Therefore, the multilayer printed circuit board having the IVH structure is free from a necessity of specially forming regions for forming the through holes. Therefore, arbitrary layers can freely be connected to one another through small via holes. As a result, size reduction, high density and high-speed propagation of signals can be easily realized.

[0006] The multilayer printed circuit board having the IVH structure is manufactured by a process arranged, for example, as shown in Fig. 6.

[0007] Initially, a material having a structure in which an aramide nonwoven fabric cloth is impregnated with epoxy resin is employed as prepreg 112. Then, an operation for forming holes in the prepreg 112 is performed by using carbon dioxide gas laser. Then, conductive paste 114 is enclosed in obtained hole portions 112a (see Fig. 6 (A)).

[0008] Then, copper foil 116 is laminated on each of the two sides of the prepreg 112, and then heat and pressure are applied to the prepreg 112 having the copper foil 116 by heat pressing. Hence it follows that the epoxy resin and the conductive paste of the prepreg 112 are hardened so that the electrical connection between the two copper foil members 116 on the two sides of the prepreg 112 is established (see Fig. 6 (B)).

[0009] Then, the copper foil 116 on each side is patterned by an etching method so that a hard and double-sided substrate having via holes is obtained (see Fig. 6 (C)).

[0010] Then, the obtained double-sided substrates are used as core layers to form a multilayer structure. Specifically, the prepreg and copper foil are sequentially laminated on the two sides of the foregoing core layer while the prepreg and the copper foil are being aligned. Then, heat pressing is again performed, and then the uppermost copper foil 116 is etched. Thus, a four-layer substrate is obtained (see Figs. 6 (D) and 6 (E)). When a structure having a large number of layers is formed, the foregoing process is repeated. Thus, a six-layer substrate or an eight-layer substrate can be obtained.

[0011] The foregoing conventional technique, however, must repeat the laminating process using heat pressing and the process for patterning the copper foil by performing the etching operation. Therefore, the manufacturing process becomes too complicated and considerable time is required to complete the manufacturing operation.

[0012] If the multilayer printed circuit board having the IVH structure which can be obtained by the above-mentioned manufacturing method encounters only one defective portion (only one defective process) in the patterning operation during the manufacturing process, the overall circuit board, which is the final product, becomes a defective product. Hence it follows that the manufacturing yield deteriorates excessively.

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[0013] To overcome the above-mentioned problems, an object of the present invention is to provide a high-density multilayer printed circuit board having the IVH structure which can be manufactured by a very simple process and which permits a satisfactory high manufacturing yield to be realized and a manufacturing method therefor.

Disclosure of the Invention

[0014] To achieve the above-mentioned object, the present invention is structured as follows.

[0015] According to one aspect of the present invention, there is provided a method of manufacturing a multilayer printed circuit board comprising the steps (1) to (5):

(1) a step for forming a non-penetrating hole in an insulating base member, such as an organic insulating base member, having a metal layer formed on either surface thereof by a laser irradiation operation such that the non-penetrating hole reaches the metal layer;
(2) a step for forming via holes by enclosing a conductive material into the non-penetrating hole formed in step (1);
(3) a step for forming a conductive circuit by etching the metal layer;
(4) a step for forming projecting conductors on the surfaces of the via holes to form a single-sided circuit substrate;
(5) a step for laminating the single-sided circuit substrate and another single-sided circuit substrate or the single-sided circuit substrate and another substrate obtained in the steps (1) to (4) such that the projecting conductors of the single-sided circuit substrate and a conductive circuit of the other circuit are positioned opposite to each other through non-hardened resin which is an organic adhesive layer and applying heat and pressure to (heat-pressing) the laminate.

[0016] According to another aspect of the present invention, there is provided a method of manufacturing a multilayer printed circuit board comprising the steps (1) to (4):

(1) a step for forming a non-penetrating hole in an insulating base member, such as an organic insulating base member having a metal layer formed on either surface thereof by a laser irradiation operation such that the non-penetrating hole reaches the metal layer;
(2) a step for forming via holes by enclosing a conductive material into the non-penetrating hole formed in step (1) and forming projecting conductors on the surfaces of the via holes;
(3) a step for forming a conductive circuit by etching the metal layer;
(4) a step for laminating the single-sided circuit substrate and another single-sided circuit substrate or the single-sided circuit substrate and another substrate such that the projecting conductors of the single-sided circuit substrate and a conductive circuit of the other single-sided circuit substrate or the other conductive circuit are positioned opposite to each other through non-hardened resin which is an organic adhesive layer and applying heat and pressure to (heat pressing) the laminate.

[0017] In the foregoing aspects of the present invention, the projecting conductors are inserted into the non-hardened resin so that resin is squeezed out. That is, the projecting conductors penetrate the organic adhesive layer so as to be electrically connected to another substrate.

[0018] According to another aspect of the present invention, there is provided a multilayer printed circuit board obtainable from the above-mentioned manufacturing process.

[0019] That is, a multilayer printed circuit board having a structure that single-sided circuit substrates each of which has a conductive circuit formed on either side of an organic insulating base member thereof and via holes formed in the organic insulating base member by enclosing a conductive material are connected to other substrates each having a conductive circuit through organic adhesive layers, the multilayer printed circuit board comprising: projecting conductors formed on the surfaces of the via holes opposite to the surface of the organic insulating base member on which the conductive circuit is formed, wherein the projecting conductors are inserted to penetrate the adhesive layers so as to be connected to the conductive circuits of the other substrates.

[0020] The multilayer printed circuit board and a manufacturing method therefor according to the present invention are arranged such that the single-sided circuit substrates each having a conductive circuit which incorporates a predetermined wiring pattern formed thereon are previously and individually manufactured. Therefore, inspection for detecting whether or not the conductive circuit or the like has a defective portion can be performed before the single-sided circuit substrates are laminated. Hence it follows that only single-sided circuit substrates free from any defect can be used in the laminating process. That is, the manufacturing method according to the present invention is able to reduce defects in the manufacturing process. As a result, the multilayer printed circuit board having the IVH structure can be manufactured with a high manufacturing yield.

[0021] The method of manufacturing a multilayer printed circuit board according to the present invention is not

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required to repeat the heating press operation while the prepreg is being laminated as distinct from the conventional technique. That is, the present invention enables the heat pressing operation to be completed at a time such that a plurality of the single-sided circuit substrates are laminated through the adhesive agents placed on the single-sided circuit substrates. Therefore, the manufacturing method according to the present invention is free from a necessity for repeating the laminating process, in which the complicated heat press is performed, and the patterning process. Hence it follows that the multilayer printed circuit board having the IVH structure can be efficiently manufactured.

[0022] In the present invention, formation of the non-penetrating holes in the organic insulating substrate is performed by laser machining. The structure of the present invention is able to eliminate the necessity of forming holes in the organic adhesive agent by performing a laser process. That is, after holes have been formed in the organic insulating substrate by performing the laser process, the organic adhesive layer can be formed on the single-sided circuit substrate or the substrate having the conductor circuit.

[0023] That is, the present invention is structured such that the projecting conductors inserted into the organic adhesive layer during the heat pressing establish the connection of the conductor circuits. Therefore, previous formation of the conducting hole in the organic adhesive layer is not required.

The organic adhesive layer may be formed at the final heat pressing process. As a result, the desmear process, which is performed after the hole has been formed in the process for manufacturing the single-sided circuit substrate, may be performed before the formation of the organic adhesive layer. Hence it follows that the desmear process does not erode the organic adhesive layer.

[0024] Also in a case where the non-penetrating hole is filled with the electrolytic plating, the organic adhesive layer can be formed on the single-sided circuit substrate or the substrate having the conductive circuit after the non-penetrating hole has been formed in the organic insulating base member by performing the laser process and the non-penetrating hole has been filled with the electrolytic plating. Therefore, the electrolytic plating solution and the organic adhesive layer are not made contact with each other. As a result, the erosion and contamination of the organic adhesive layer with the plating solution can be prevented.

[0025] Since the organic adhesive layer is not hardened until the heat pressing process which is the final process is performed, the organic adhesive layer easily deteriorates owing to the desmear process and the plating solution. The present invention is characterized in that the foregoing problem can be prevented and a reliable substrate can easily be formed.

[0026] Moreover, a necessity for previously forming a conducting hole in the adhesive layer can be eliminated. Therefore, defective conduction caused from deviation in the positions of the hole in the adhesive layer and the projecting conductors provided for the organic insulating base member can be prevented.

[0027] In the present invention, the projecting conductors are formed on the via holes filled with the conductive paste or the electrolytic plating. Therefore, electrical connection between the upper and lower conductive layers can be easily established by penetrating the relatively thin organic adhesive layer. Therefore, the height and the diameter of each projecting conductor can be reduced. Hence it follows that the pitch between adjacent projecting conductors can be shortened. Therefore, the pitch between adjacent via holes can also be shortened. As a result, addressing to raising of the density can be permitted.

[0028] In a case where the via holes are filled with the electrolytic plating, the resistance value between the upper and the lower conductor layers can be lowered.

[0029] Techniques for connecting the upper and lower conductors to each other by penetrating the resin insulating layer have been disclosed in Japanese Patent Laid-Open No. 7-14628, Japanese Patent Laid-Open No. 7-106756, Japanese Patent Laid-Open No. 7-231167, Japanese Patent Laid-Open No. 8-172270 and Japanese Patent Laid-Open No. 8-288649. The foregoing techniques are different from the technique with which the projecting conductors formed on the via holes filled with the foregoing material are caused to penetrate only the organic adhesive layer to connect the upper and lower conductors to each other. Therefore, the effect of the present invention cannot be obtained.

Brief Description of Drawings

[0030]

Fig. 1 is a vertical cross sectional view showing a multilayer printed circuit board according to an embodiment of the present invention;

Fig. 2 is a diagram showing a process for manufacturing a core substrate which constitutes the multilayer printed circuit board according to the embodiment of the present invention;

Fig. 3 is a diagram showing a process for manufacturing a single-sided circuit substrate which constitutes the multilayer printed circuit board according to the embodiment of the present invention;

Fig. 4 is a diagram showing a process for manufacturing the single-sided circuit substrate which constitutes the multilayer printed circuit board according to the embodiment of the present invention;

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Fig. 5 is a diagram showing a process for manufacturing the multilayer printed circuit board according to the embodiment of the present invention;

Fig. 6 is a diagram showing a process for manufacturing a conventional multilayer printed circuit board;

Fig. 7 is a diagram showing a process for manufacturing the core substrate which constitutes the multilayer printed circuit board according to the embodiment of the present invention;

Fig. 8 is a diagram showing a process for manufacturing the core substrate which constitutes the multilayer printed circuit board according to the embodiment of the present invention; and

Fig. 9 is an enlarged photograph showing a metal structure of the cross section of a via hole in the multilayer printed circuit board according to the embodiment of the present invention.

Best Mode for Carrying Out the Invention

[0031] A multilayer printed circuit board and a manufacturing method therefor according to an embodiment of the present invention will now be described with reference to the drawings.

[0032] Fig. 1 shows a vertical cross section of a multilayer printed circuit board having a full-thickness IVH structure according to the embodiment of the present invention. A multilayer printed circuit board 10 is a multilayer printed circuit board incorporating a core substrate 20 disposed in a central portion of the multilayer printed circuit board 10 and single-sided circuit substrates 30A, 30B, 30C and 30D, two substrates of which are formed on the upper surface of the core substrate 20 and the lower surface of the same, respectively.

[0033] Conductive circuits 32a, 32b, 32c and 32d each having a predetermined pattern are formed on the surfaces of the corresponding single-sided circuit substrates 30A, 30B, 30C and 30D. Adhesive layers 34 are formed on other surfaces of the same. The core substrate 20 and the single-sided circuit substrates 30A, 30B, 30C and 30D are bonded to one another through the adhesive layers 34. The single-sided circuit substrates 30A, 30B, 30C and 30D have corresponding via holes 36a, 36b, 36c and 36d formed by enclosing electrolytic copper plating. Projecting conductors (hereinafter called "bumps") 38a, 38b, 38c and 38d made of metal, such as solder or an indium alloy or conductive paste, are formed on the foregoing via holes (the surfaces of the via holes opposite to the surfaces on which the conductive circuits are formed).

[0034] That is, in the multilayer printed circuit board 10, a conductive circuit 32a of the lowermost single-sided circuit substrate 30A is connected to a bump 38a through the via hole 36a. The bump 38a is made contact with a conductive circuit 32b of the single-sided circuit substrate 30B to establish the connection between the two circuits. The bump 38b connected to the conductive circuit 32b through the via hole 36b is made contact with the via hole 24 of the core substrate 20 so that conduction is realized. The via hole 24 of the core substrate 20 is connected to the bump 38c of the upper single-sided circuit substrate 30C. The conductive circuit 32c connected to the bump 38c through the via hole 36c is connected to the bump 38d of the uppermost single-sided circuit substrate 30D. The bump 38d is connected to the conductive circuit 32d through the via hole 36d. An electronic element, such as a bear chip, can be mounted on either surface or two surfaces of the uppermost single-sided circuit substrate 30D. Thus, the conductive circuit 32a of the lowermost single-sided circuit substrate 30A of the multilayer printed circuit board and the chip element (not shown) mounted on the conductive circuit 32 of the uppermost single-sided circuit substrate 30D are connected to each other through the via holes 36a, 36b, 36c and 36d. The foregoing via holes constitute interstitial via holes.

[0035] The method of manufacturing the multilayer printed circuit board 10 will now be continued. A method of manufacturing the core substrate 20 will now be described with reference to Fig. 2.

[0036] The core substrate may be a known rigid substrate, such as an epoxy resin substrate having a glass cloth base member or a BT (Bismaleimide-Triazine) resin substrate having a glass cloth base member.

[0037] Specifically, in process (A) shown in Fig. 2, a starting material is copper-clad laminates incorporating a substrate 22 which is made of BT (Bismaleimide-Triazine) resin and which has two sides on each of which copper foil 21 is bonded. In process (B), holes 22a serving as through holes are formed in the substrate 22 by punching, and then electroless plating is performed so that the inner surfaces of the holes 22a are applied with copper plating. Thus, via holes 24 are formed.

[0038] In process (C), etching resist (not shown) is previously applied, and then an etching process is performed to remove unnecessary portions of the copper foil 21. As a result, a predetermined conductive circuit 25 is formed.

[0039] In process (D), the surfaces of the conductive circuit 25 and the through holes 24 are subjected to blacking-reducing process so as to be coarsened.

[0040] In process (E), resin 26 which must be enclosed is uniformly applied by using a roll coater, and then the resin which must be enclosed is hardened. Then, the resin which must be enclosed is ground with a belt sander or the like until the conductive circuit 25 is exposed on the surface. As a result, a core substrate 20 having two flat surfaces is manufactured.

[0041] The core substrate 20 is brought to a state in which the inside portion of the through holes 24 and two sides 25a of the conductive circuit 25 are coarsened. As a result, the adhesiveness between the conductive circuit 25 and the

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resin 26 which must be enclosed can be improved. Hence it follows that occurrence of a crack can be prevented which occurs in the adhesive layer 34 described with reference to Fig. 1 and which starts at the interface between the conductive circuit 25 and the resin 26 which must be enclosed.

[0042] Description of the method of manufacturing the single-sided circuit substrate 30 will now be continued with reference to Figs. 3 and 4. In process (A) shown in Fig. 3, an insulating base member 40 having a metal layer 42 formed on either surface thereof is used as a starting material. The insulating base member 40 must be an organic insulating base member. Specifically, it is preferable that a base member is selected from rigid laminates including an aramide nonwoven fabric cloth-epoxy resin base member, a glass cloth epoxy resin base member, an aramide nonwoven fabric cloth-polyimide base member and a bismaleimide-triazine resin base member or films including a polyphenylene (PPE) film and a polyimide (PI) film.

[0043] It is preferable that the insulating base member 40 is a rigid laminated base member. In particular, it is preferable that a single-sided circuit substrate is employed. The reason for this lies in that displacement of the positions of the wiring pattern and the via holes can be prevented during handling which is performed after the metal layer 42 has been etched. That is, excellent accuracy of the position can be realized.

[0044] The metal layer 42 formed on the insulating base member 40 may be copper foil. The copper foil may be subjected to a matting process in order to improve the adhesiveness. The single-sided circuit substrate is a substrate which can be obtained by heat-pressing a laminate of prepreg and copper foil, the prepreg being in the form of a B-stage constituted by causing a glass cloth to be impregnated with thermosetting resin, such as epoxy resin, phenol resin or bismaleimide-triazine resin. The single-sided circuit substrate is a rigid substrate which can easily be handled and which is an advantage substrate from the viewpoint of cost reduction. Metal may be evaporated on the surface of the insulating base member 40, followed by forming a metal layer by performing electrolytic plating.

[0045] The thickness of the insulating base member 40 is 10 μm to 200 μm, preferably 15 μm to 100 μm. The optimum thickness is 20 μm to 80 μm to maintain insulating characteristics. If the thickness is smaller than the above-mentioned ranges, the strength is decreased excessively to perform easy handling. If the thickness is too large, formation of small via holes is inhibited and enclosing of the conductive material cannot easily be performed.

[0046] The thickness of the metal layer 42 is 5 μm to 35 μm, preferably 8 μm to 30 μm, and more preferably 12 μm to 25 mm. If the thickness is too small, a hole attempted to be formed by a laser process as described later is undesirably formed into a through hole. If the thickness is too large, a fine pattern cannot be formed by the etching process.

[0047] Then, the laser irradiation process is performed to form non-penetrating holes 40a in the insulating base member 40 (process (B)). The laser processing machine may be a carbon dioxide gas laser processing machine, an UV laser processing machine or an excimer laser processing machine. It is preferable that the caliber of the laser processing machine is 20 μm to 150 μm. The carbon dioxide gas laser processing machine exhibits high processing speed, enabling the cost of the process to be reduced. Therefore, the foregoing laser processing machine is a most suitable machine from a viewpoint of industrial use. Therefore, the foregoing laser processing machine is a most suitable machine for the present invention. When the carbon dioxide gas laser processing machine is employed, resin existing in the non-penetrating hole 40a and slightly melted onto the surface of the metal layer 42 is easily left. Therefore, it is preferable that a desmear process is performed to maintain the reliability of the connection.

[0048] Then, a conductive material 46 is enclosed in the non-penetrating holes 40a formed by the laser process so that via holes 36a are formed (process (E)). The conductive material 46 can be enclosed by electrolytic plating or electroless plating. As an alternative to this, conductive paste may be enclosed or a portion of electrolytic plating or electroless plating may be enclosed, followed by enclosing conductive paste into a residual portion. The conductive paste may be conductive paste made of metal particles made of one or more materials selected from silver, copper, gold, nickel and solder. As the metal particles, a material may be employed which is obtained by coating the surfaces of the metal particles with different metal. Specifically, metal particles may be employed which are obtained by coating the surfaces of copper particles with noble metal selected from gold and silver.

[0049] It is preferable that the conductive paste is organic conductive paste obtained by adding thermosetting resin, such as epoxy resin or polyphenylene sulfide (PPS), to the metal particles.

[0050] In this embodiment, the small holes each having a diameter of 20 μm to 150 μm are formed by the laser process. Since the foregoing holes are non-penetrating holes, the conductive paste cannot reliably be enclosed because air bubbles are easily left. Therefore, the electrolytic plating is a preferred means from a viewpoint of practical use. The electrolytic plating may be, for example, copper, gold, nickel or solder plating. Most suitable electrolytic plating is copper electrolytic plating.

[0051] When the electrolytic plating is employed to perform the enclosure, the metal layer 42 formed on the organic insulating base member 40 is used as the lead for the electrolytic plating. Since the metal layer 42 is formed on the overall surface of the organic insulating base member 40, the density of the electric field can be uniformed. Therefore, the non-penetrating holes can be enclosed with the electrolytic plating such that a uniform height is realized. It is preferable that the surface of the metal layer 42 in each of the non-penetrating holes 40a is subjected to an activating process using acid or the like. When plating is performed, it is preferable that deposition of the electrolytic plating on the surface

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of the metal layer 42 provided for the organic insulating base member 40 is prevented by applying a mask 48 on the metal layer 42 in process (C). As an alternative to this, in process (D), two insulating base members 40 are laminated and brought into hermetic contact with each other to prevent contact with the plating solution during the electrolytic plating process.

[0052] After the electrolytic plating has been completed, a portion of the electrolytic plating (metal 46) projecting over the non-penetrating holes 40a may be removed by grinding or the like to flatten the surface in process (F) shown in Fig. 4. The grinding process may be performed by using a belt sander or by buffing.

[0053] In process (G), a process which is performed before the metal layer 42 is etched to form the conductive circuit and which is a process for easily forming a fine pattern is carried out with which the non-penetrating holes are previously formed by a laser process, followed by etching the overall surface of the metal layer 42 to reduce the thickness to about 1 μm to about 10 μm, preferably about 2 μm to about 8 μm.

[0054] As shown in process (H), a mask having a predetermined pattern is applied, and then the metal layer 42 is etched to form the conductive circuit 32a. Initially, a photosensitive dry film is applied or liquid-type photosensitive resist coat is applied. Then, exposure and development are performed to conform to the predetermined circuit pattern so that an etching resist is formed. Then, the metal layer in the portions in which the etching resist is not formed is etched so that a conductor pattern is formed. It is preferable that the etching is performed by using solution of at least one type of material selected from sulfuric acid-hydrogen peroxide, persulfate, cupric chloride and ferric chloride.

[0055] Note that the uppermost pattern may be formed by etching the metal layer after the heat pressing process has been completed. When the metal layer is etched after the heat pressing process has been completed, an advantage can be realized in that heat pressing can be performed with uniform pressure because the surfaces which must be pressed are flat surfaces.

[0056] It is preferable that the surface of the conductive circuit 32a is subjected to a coarsening process. The reason for this lies in that the adhesiveness with the adhesive layer 34 described with reference to Fig. 1 can be improved in the foregoing case to prevent separation (delamination). The coarsening process may be, for example, a soft etching process, a blackening (oxidizing)-reducing process, formation of needle-shape alloy plating ("INTERPLATE" which is trade name of Ebara) of copper-nickel-phosphorus or surface coarsening process using etching solution "MECH ETCH-BOND" which is trade name of Mech.

[0057] In process (I), bumps 38a are formed on the surfaces of the via holes 36a opposite to the surface on which the conductive circuit 32a has been formed. The bumps 38a can be formed by, for example, a method with which conductive paste is screen-printed by using a metal mask having openings formed at predetermined positions, a method with which paste of solder which is metal having a low melting point is printed, a method with which solder plating is performed or a method with which immersion in solution in which solder has been melted is performed.

[0058] The metal having the low melting point may be Pb-Sn type solder, Ag-Sn type solder or indium solder.

[0059] It is preferable that the height of each bump is 3 μm to 60 μm. If the height is smaller than 3 μm, absorption of dispersion of the heights of the bumps by virtue of deformation of the bumps cannot be realized. If the height is larger than 60 μm, the resistance value is raised excessively. What is worse, the bumps are expanded in the lateral direction when the bumps have been deformed, causing short circuit to occur.

[0060] When the conductive paste is enclosed in the non-penetrating holes 40, formation of the bumps can be performed simultaneously with the enclosure. In the foregoing state or before the bump are formed, inspections of the conductive circuit 32a and the via holes 36a can be performed. The conventional multilayer printed circuit board permits the inspection of the conductive circuit to be performed only after lamination has been performed, that is, after completion. As compared with this, whether or not the single-sided circuit substrate 30A has a defect can be inspected before the laminating operation. Since only single-sided circuit substrate 30A free from any defect can be used in a laminating process to be described later, a satisfactory high yield of the multilayer printed circuit board can be obtained.

[0061] Finally, in process (J), the overall surface of the insulating base member 40 adjacent to the bumps 38a or the overall surface of the insulating base member 40 adjacent to the conductive circuits 25, 32b and conductive circuit 32c is coated with resin. Then, the resin is dried so that an adhesive layer 34 constituted by non-hardened resin is formed.

[0062] The adhesive layer 34 may be formed by coating the overall surface of the single-sided circuit substrate on which the conductive circuit has been formed, the overall opposite surface or the overall surface of substrate 20 on which the conductive circuit 32b has been formed, the substrate 20 being a substrate having a conductive circuit. Therefore, a necessity for forming holes for establishing conduction in the adhesive layer can be eliminated. It is preferable that the adhesive layer 34 is made of organic adhesive agent. It is preferable that the organic adhesive agent is a resin selected from epoxy resin, polyimide resin, thermosetting polyphenylene ether (PPE), composite resin of the epoxy resin and the thermosetting resin, composite resin of epoxy resin and silicon resin or BT resin.

[0063] The non-hardened resin which is the organic adhesive agent can be applied by using a curtain coater, a spin coater, a roll coater or a spray coater or by screen printing. Also the formation of the adhesive layer can be performed by laminating an adhesive sheet. It is preferable that the thickness of the adhesive layer is 5 μm to 50 μm. To facilitate

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handling, it is preferable that the adhesive layer is pre-cured.

[0064] The process of laminating the core substrate 20 described with reference to Fig. 2 and the single-sided circuit substrate 30 described with reference to Figs. 3 and 4 will continuously be described with reference to Fig. 5.

[0065] In process (K), the single-sided circuit substrate 30A, the single-sided circuit substrate 30B, 30C and 30D formed by a process similar to the above-mentioned process and the core substrate 20 are laminated. All of the single-sided circuit substrates 30A, 30B, 30C and 30D and the core substrate 20 must be substrates subjected to inspection for a defective portion. Initially, the single-sided circuit substrate 30B is placed on the organic adhesive layer 34 of the single-sided circuit substrate 30A, while the core substrate 20 is placed on the organic adhesive layer 34 of the single-sided circuit substrate 30B. The foregoing substrate are laminated on the core substrate in such a manner that the single-sided circuit substrates 30C and 30D are inverted, that is, the organic adhesive layer 34 of the single-sided circuit substrate 30C faces the core substrate 20. Moreover, the organic adhesive layer 34 of the single-sided circuit substrate 30D faces the single-sided circuit substrate 30C. The lamination is performed while position alignment is being performed by inserting a guide pin (not shown) into a guide hole (not shown) formed around the single-sided circuit substrate 30 and the core substrate 20. A portion of circle C of the laminated substrate shown in the drawing is indicated by enlarging the same in (M). The position alignment may be performed by an image process.

[0066] Finally, in process (L), the laminated substrates are heated to 150°C to 200°C by using a heating press and applied with pressure of 5 kgf/cm^2 to 100 kgf/cm^2, preferably 20 kgf/cm^2 to 50 kgf/cm^2. Thus, the single-sided circuit substrates 30A, 30B, 30C and 30D and the core substrate 20 are integrated into a multilayer structure by one press molding operation. A portion of circle C of the laminated substrates shown in the drawing is shown in (N). Since the pressure is applied, the bump 38a of the single-sided circuit substrate 30A squeezes out the non-hardened resin (the insulating resin) existing between the bump 38a and the conductive circuit 32b adjacent to the single-sided circuit substrate 30B. Thus, the bump 38a is brought into contact with the conductive circuit 32b so that the connection between the bump 38a and the conductive circuit 32b is established. Similarly, the bumps 38b, 38c and 38d of the single-sided circuit substrate 30B, 30C and 30D and the conductive circuit are connected to one another. Since also heat is applied simultaneously with exertion of the pressure, the adhesive layer 34 of the single-sided circuit substrate 30A is hardened so that strong adhesion is realized with the single-sided circuit substrate 30B. It is preferable that the heating press is vacuum heating press. As a result, the multilayer printed circuit board 10 described with reference to Fig. 1 can be manufactured.

[0067] Another embodiment will now be described with reference to Figs. 7 to 9.

[0068] In process (B), a protective film 100 which is usually used as a mask serving in a process for printing conductive paste is bonded to a single-sided copper-clad laminate 40 which has been prepared in process (A) shown in Fig. 7. In process (C), an operation for laser-processing the single-sided copper-clad laminate 40 is performed so that non-penetrating holes 40a are formed. The protective film 100 may be a Mylar film or a release sheet. For example, a polyethylene terephthalate film (PET) having an adhesive layer formed on the surface thereof may be employed. Then, deposition of plating onto the metal layer 42 must be prevented by bonding a mask 48 in process (D). As an alternative to this, the metal layers 42 are brought into hermetic contact with each other in process (E) to prevent contact with the electrolytic plating solution. In process (F) a portion of the non-penetrating holes is filled with electrolytic plating 46. In process (G) conductive paste 460 is enclosed in residual spaces. In the foregoing embodiment, dispersion of the heights of the electrolytic plating can be corrected by using conductive paste so that the heights of the bumps are uniformed.

[0069] An average charging rate of the electrolytic plating in the non-penetrating holes (heights t of electrolytic plating × 100/depth T of the non-penetrating holes : refer to (L) to Fig. 8 (L) which is an enlarged view of portion C shown in Fig. 8 (I)) is not lower than 50 % and lower than 100 %, preferably 55 % to 95 %.

[0070] The conductive paste enclosed in the opening portions of the protective film 100 is formed into bumps. In process (H) a film 101 for protecting the conductive paste is bonded. Then, the metal layer 42 is etched so that a conductive circuit 32a is formed. Then, the films 100 and 101 are removed to expose the bumps so that a single-sided circuit substrate 30E is obtained (refer to process (I)).

[0071] It is preferable that the bumps made of the conductive paste is in a semi-hardened state. Since the conductive paste is hard if it is in the semi-hardened state, the conductive paste is able to penetrate the organic adhesive layer softened during the heat pressing process. When the heat pressing process is performed, the conductive paste is deformed, causing the area of contact to be enlarged. As a result, the conduction resistance can be lowered and dispersion of the heights of the bumps can be corrected. Fig. 9 shows an enlarged photograph of the structures of the via hole and the bump portion.

[0072] Then, an organic adhesive agent 80 is applied to the single-sided circuit substrate 30E obtained by performing steps (A) to (I). Then, in process (J), three layers for each side are placed opposite to each other through the adhesive layers. The lamination is performed while position alignment is being performed by inserting a guide pin (not shown) into a guide hole (not shown) formed in the peripheries of the single-sided circuit substrate 30 and the core substrate 20. The position alignment may be performed by performing an image process.

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[0073] Then, the multilayer printed circuit board 10 structured in process (K) may be manufactured by performing heat pressing.

[0074] In the foregoing embodiment, the multilayer printed circuit boards have four laminated single-sided circuit substrates 30 and six laminated single-sided circuit substrates 30, respectively. The structure according to the present invention may be applied to a multilayer printed circuit board having three layers or five or more layers. The single-sided circuit substrates according to the present invention may be laminated on a single-sided printed circuit board, a double-sided printed circuit board, a double-sided through-hole printed circuit board or a multilayer printed circuit board to manufacture a multilayer printed circuit board.

[0075] Although the foregoing embodiment has the structure that the holes for forming the via holes are formed by the laser process, the holes may be formed by a mechanical method, such as drilling, punching or the like.

[0076] The multilayer printed circuit board according to the present invention may be subjected to a variety of usual processes to which the printed circuit board has been subjected. For example, formation of solder resist on the surface, nickel/gold plating, soldering, hole formation, a cavity forming process and plating of through holes may be performed.

[0077] As described above, the multilayer printed circuit board and a manufacturing method therefor according to the present invention are arranged such that the single-sided circuit substrates each having a conductive circuit which incorporates a predetermined wiring pattern formed thereon are previously and individually manufactured. Therefore, inspection for detecting whether or not the conductive circuit or the like has a defective portion can be performed before the single-sided circuit substrates are laminated. Hence it follows that only single-sided circuit substrates free from any defect can be used in the laminating process. That is, the manufacturing method according to the present invention is able to reduce defects in the manufacturing process. As a result, the multilayer printed circuit board having the IVH structure can be manufactured with a high manufacturing yield.

[0078] The method of manufacturing a multilayer printed circuit board according to the present invention is not required to repeat the heating press operation while the prepreg is being laminated as distinct from the conventional technique. That is, the present invention enables heat pressing operation to be completed at a time such that a plurality of the single-sided circuit substrate are laminated through the adhesive agents placed on the single-sided circuit substrates. Therefore, the manufacturing method according to the present invention is free from a necessity for repeating the laminating process in which the complicated heat press is performed and the patterning process. Hence it follows that the multilayer printed circuit board having the IVH structure can efficiently be manufactured. Since the single-sided circuit substrates are integrated with physical force exerted in one time of the pressing operation, the reliability of the connection can be improved.

[0079] In the present invention, formation of the non-penetrating hole in the organic insulating base member is performed by the laser process. In the present invention, the previous formation of the conducting hole in the organic adhesive layer is not required. The necessity for simultaneously forming holes in the insulating base member and the adhesive layer by the laser process can be eliminated. That is, after the holes have been formed in the insulating base member by the laser process, the adhesive layer can be formed on the single-sided circuit substrate or the substrate having the conductive circuit. Therefore, the desmear process, which is performed after the holes have been formed can be performed before the adhesive layer is formed. As a result, the desmear process does not erode the organic adhesive layer.

[0080] Also in a case where the non-penetrating hole is filled with the electrolytic plating, the adhesive layer can be formed on the single-sided circuit substrate or the substrate having the conductive circuit after the non-penetrating hole has been formed in the insulating base member by performing the laser process and the non-penetrating hole has been filled with the electrolytic plating. Therefore, the electrolytic plating solution and the adhesive layer are not made contact with each other. As a result, the erosion of the adhesive layer with the plating solution can be prevented.

[0081] Since the adhesive layer is not hardened until the heat pressing process which is the final process is performed, the adhesive layer easily deteriorates during the desmear process or the plating solution. The present invention has characteristics that the above-mentioned problem can be prevented and a reliable substrate can be easily formed.

[0082] Moreover, a necessity for previously forming a conducting hole in the adhesive layer can be eliminated according to the present invention. Therefore, defective conduction caused from deviation in the positions of the hole in the adhesive layer and the projecting conductors provided for the organic insulating base member can be prevented.

[0083] In the present invention, the projecting conductors are formed on the via holes filled with the conductive paste or the electrolytic plating. Therefore, the electrical connection between the upper and lower conductive layers can be easily established by penetrating the relatively thin organic adhesive layer. Therefore, the height and the diameter of each projecting conductor can be reduced. Hence it follows that the pitch between adjacent projecting conductors can be shortened. Therefore, the pitch between adjacent via holes can also be shortened. As a result, addressing to raising of the density can be permitted.

[0084] In a case where the via holes are filled with the electrolytic plating, the resistance value between the upper and the lower conductor layers can be lowered.

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Claims

1. A multilayer printed circuit board having a structure that single-sided circuit substrates each of which has a conductive circuit formed on either side of an insulating base member thereof and via holes formed in said insulating base member by enclosing a conductive material are connected to other substrates each having a conductive circuit through adhesive layers, said multilayer printed circuit board comprising:

   projecting conductors formed on the surfaces of said via holes opposite to the surface of said insulating base member on which said conductive circuit is formed, wherein
   said projecting conductors are inserted to penetrate said adhesive layers so as to be connected to said conductive circuits of the other substrates.

2. A multilayer printed circuit board having a structure that single-sided circuit substrates each of which has a conductive circuit formed on either side of an organic insulating base member thereof and via holes formed in said organic insulating base member by enclosing a conductive material are connected to other substrates each having a conductive circuit through organic adhesive layers, said multilayer printed circuit board comprising:

   projecting conductors formed on the surfaces of said via holes opposite to the surface of said organic insulating base member on which said conductive circuit is formed, wherein
   said projecting conductors are inserted to penetrate said adhesive layers so as to be connected to said conductive circuits of the other substrates.

3. A multilayer printed circuit board according to claim 1 or 2, wherein said conductive material is electrolytic copper plating.

4. A multilayer printed circuit board according to any one of claims 1 to 3, wherein said projecting conductors are made of conductive paste or metal having a low melting point.

5. A multilayer printed circuit board according to any one of claims 1 to 4, wherein said adhesive layer is formed by coating or laminating said adhesive layer on the overall surface of said single-sided circuit substrate on which said conductive circuit has been formed, the overall surface of said single-sided circuit substrate opposite to the surface of said single-sided circuit substrate on which said conductive circuit has been formed or the overall surface of the other circuit having said conductive circuit on which said conductive circuit has been formed.

6. A method of manufacturing a multilayer printed circuit board at least comprising the steps (1) to (5):

   (1) a step for forming a non-penetrating hole in an insulating base member having a metal layer formed on either surface thereof by a laser irradiation operation such that said non-penetrating hole reaches said metal layer;
   (2) a step for forming via holes by enclosing a conductive material into said non-penetrating hole formed in step (1); (3) a step for forming a conductive circuit by etching said metal layer;
   (4) a step for forming projecting conductors on the surfaces of said via holes formed on the surface opposite to the surface on which said conductive circuit has been formed to form a single-sided circuit substrate; and
   (5) a step for laminating said single-sided circuit substrate and another substrate such that said projecting conductors of said single-sided circuit substrate and a conductive circuit of the other circuit are positioned opposite to each other through an adhesive layer and applying heat and pressure to the laminate to cause said projecting conductors to be inserted to penetrate said adhesive layer so as to be connected and integrated with said conductive circuit of the other substrate.

7. A method of manufacturing a multilayer printed circuit board at least comprising the steps (1) to (4):

   (1) a step for forming a non-penetrating hole in an insulating base member having a metal layer formed on either surface thereof by a laser irradiation operation such that said non-penetrating hole reaches said metal layer;
   (2) a step for forming via holes by enclosing a conductive material into said non-penetrating hole formed in step (1) and forming projecting conductors on the surfaces of said via holes to form a single-sided circuit substrate;
   (3) a step for forming a conductive circuit by etching said metal layer; and
   (4) a step for laminating said single-sided circuit substrate and another substrate such that said projecting con-

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ductors of said single-sided circuit substrate and a conductive circuit of the other circuit are positioned opposite to each other through an adhesive layer and applying heat and pressure to the laminate to cause said projecting conductors to be inserted to penetrate said adhesive layer so as to be connected and integrated with said conductive circuit of the other substrate.

8. A method of manufacturing a multilayer printed circuit board at least comprising the steps (1) to (5):

(1) a step for forming a non-penetrating hole in an organic insulating base member having a metal layer formed on either surface thereof by a laser irradiation operation such that said non-penetrating hole reaches said metal layer;
(2) a step for forming via holes by enclosing a conductive material into said non-penetrating hole formed in step (1); (3) a step for forming a conductive circuit by etching said metal layer;
(4) a step for forming projecting conductors on the surfaces of said via holes formed on the surface opposite to the surface on which said conductive circuit has been formed to form a single-sided circuit substrate; and
(5) a step for laminating said single-sided circuit substrate and another substrate such that said projecting conductors of said single-sided circuit substrate and a conductive circuit of the other circuit are positioned opposite to each other through an organic adhesive layer and applying heat and pressure to the laminate to cause said projecting conductors to be inserted to penetrate said adhesive layer so as to be connected to said conductive circuit of the other substrate.

9. A method of manufacturing a multilayer printed circuit board at least comprising the steps (1) to (4):

(1) a step for forming a non-penetrating hole in an organic insulating base member having a metal layer formed on either surface thereof by a laser irradiation operation such that said non-penetrating hole reaches said metal layer;
(2) a step for forming via holes by enclosing a conductive material into said non-penetrating hole formed in step (1) and forming projecting conductors;
(3) a step for forming a conductive circuit by etching said metal layer to form a single-sided circuit substrate; and
(4) a step for laminating said single-sided circuit substrate and another substrate such that said projecting conductors of said single-sided circuit substrate and a conductive circuit of the other circuit are positioned opposite to each other through an organic adhesive layer and applying heat and pressure to the laminate to cause said projecting conductors to be inserted to penetrate said organic adhesive layer so as to be connected to said conductive circuit of the other substrate.

10. A method of manufacturing a multilayer printed circuit board according to any one of claims 6 to 9, wherein said conductive material is electrolytic copper plating.

11. A method of manufacturing a multilayer printed circuit board according to any one of clams 6 to 10, wherein said projecting conductors are made of conductive paste or metal having a low melting point.

12. A method of manufacturing a multilayer printed circuit board according to any one of claims 6 to 11, wherein said adhesive layer is formed by coating or laminating said adhesive layer on the overall surface of said single-sided circuit substrate on which said conductive circuit has been formed, the overall surface of said single-sided circuit substrate opposite to the surface of said single-sided circuit substrate on which said conductive circuit has been formed or the overall surface of the other circuit having said conductive circuit on which said conductive circuit has been formed.

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Fig. 1

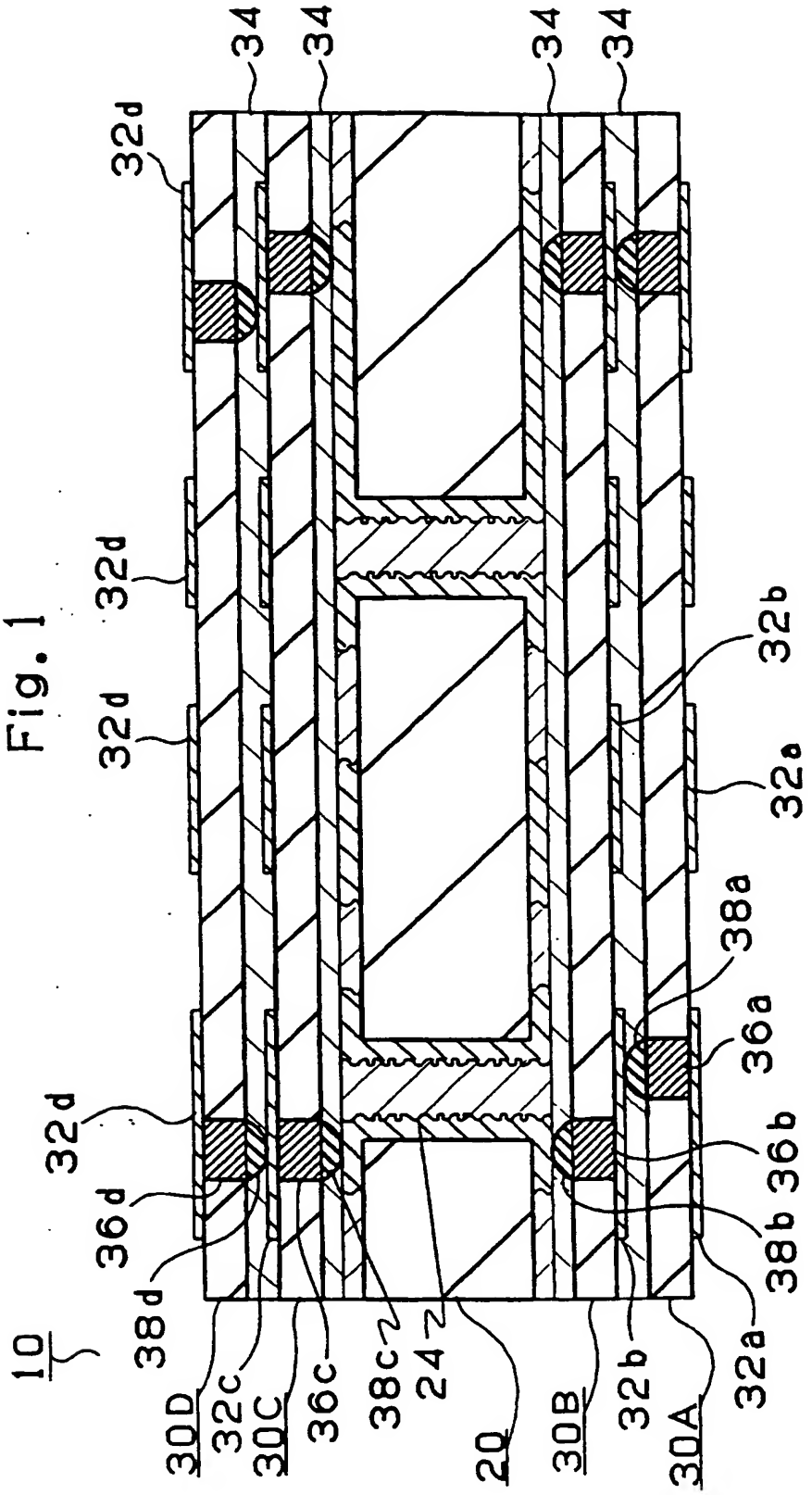

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Fig. 2

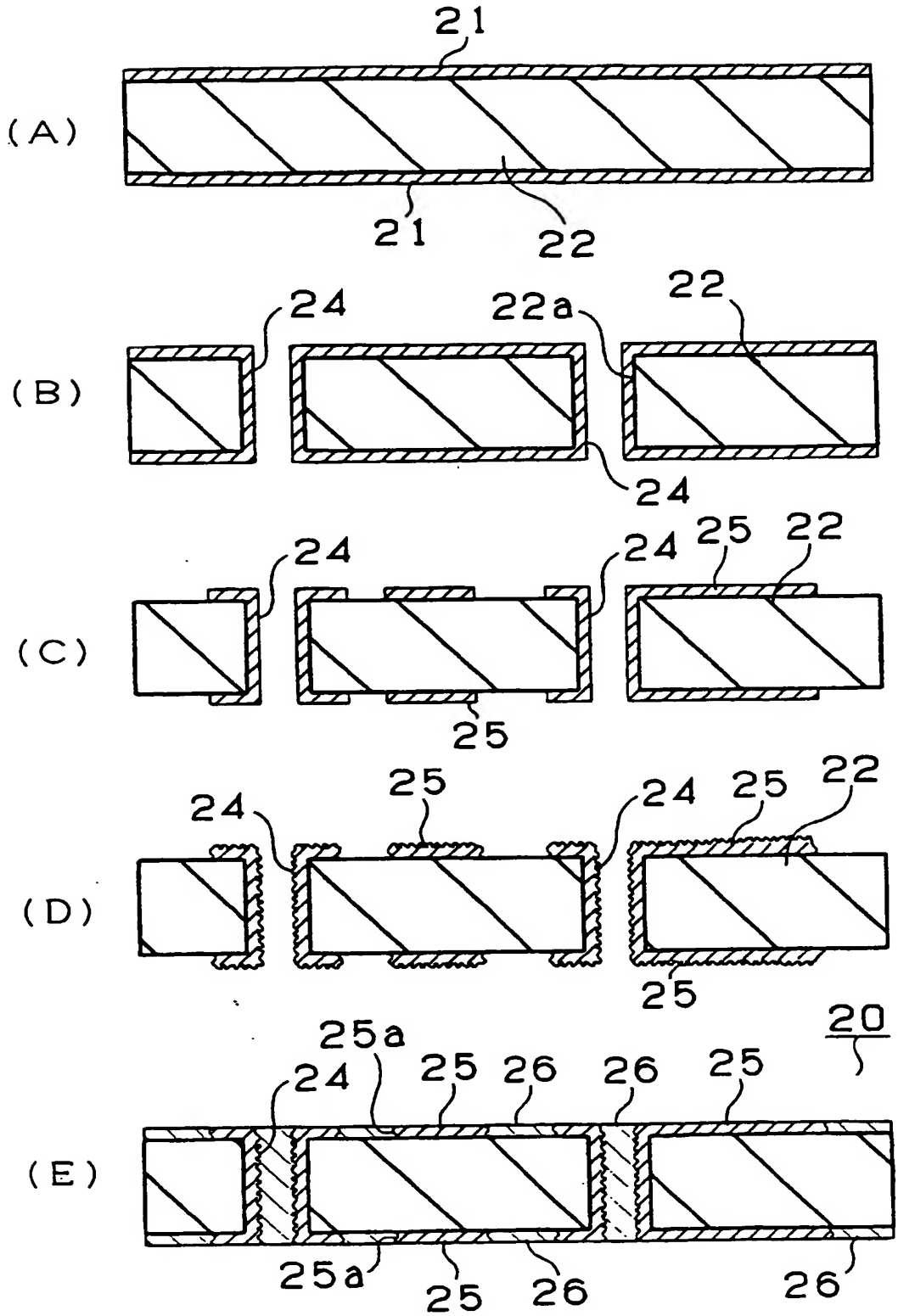

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Fig. 3

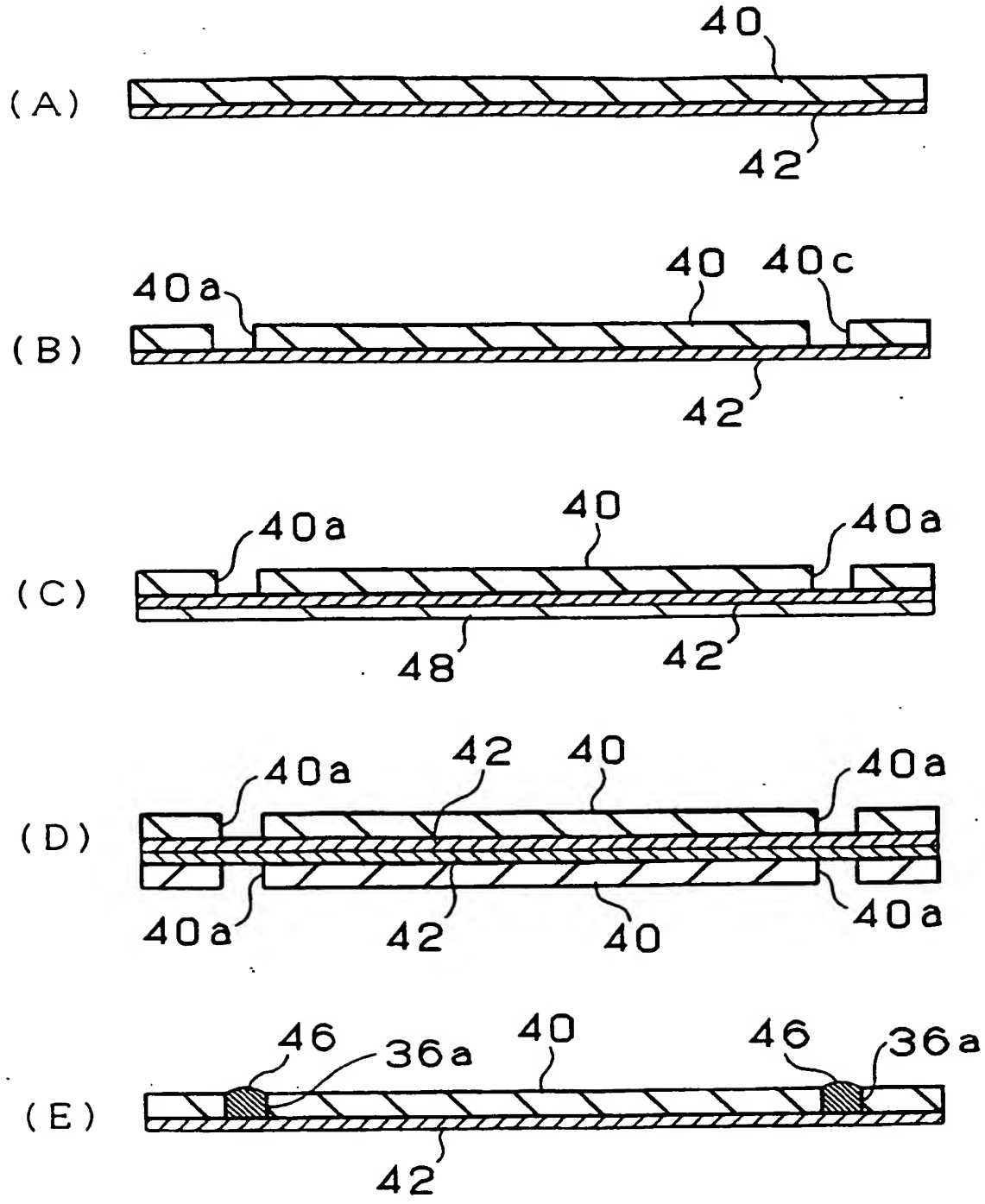

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Fig. 4

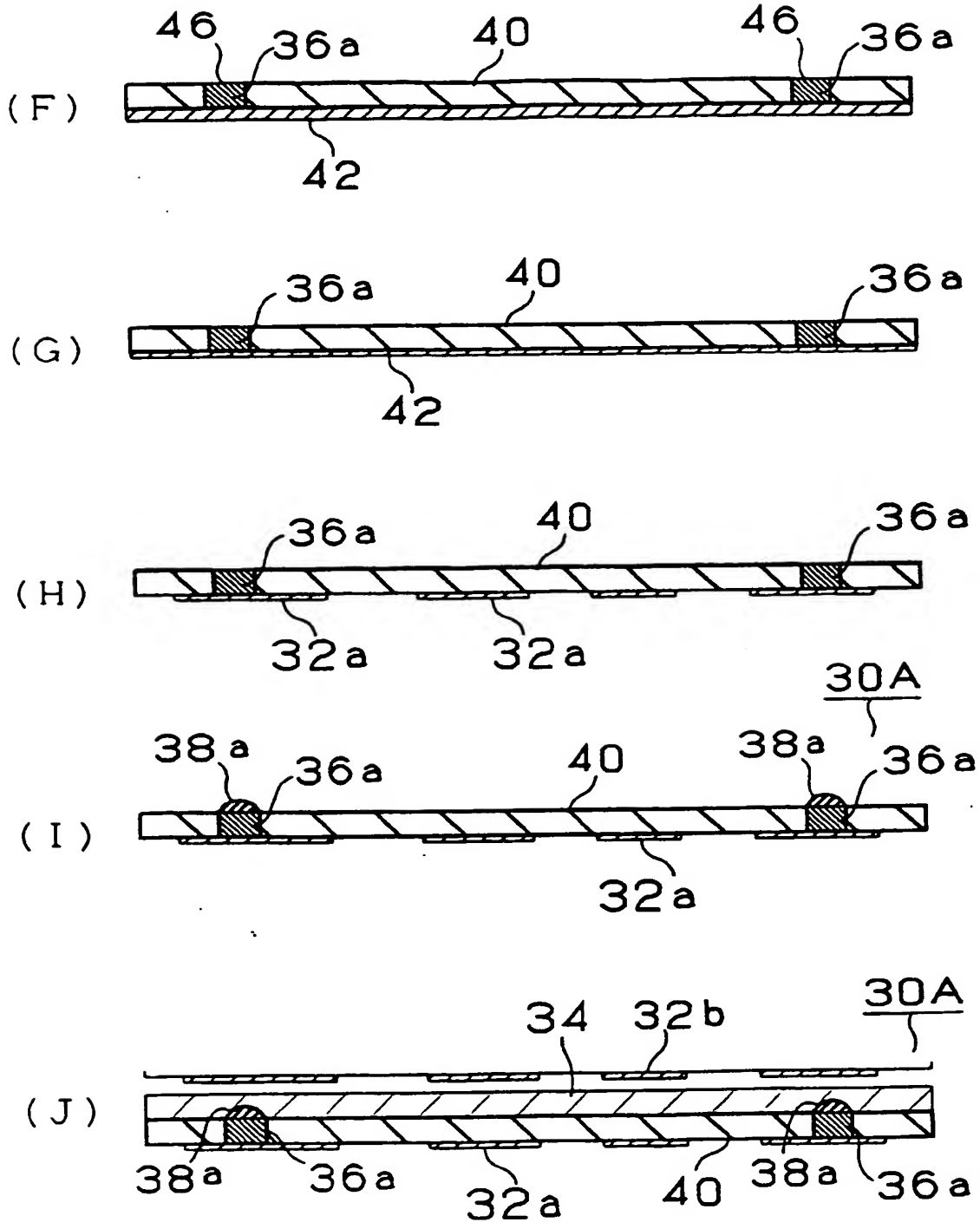

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Fig. 5

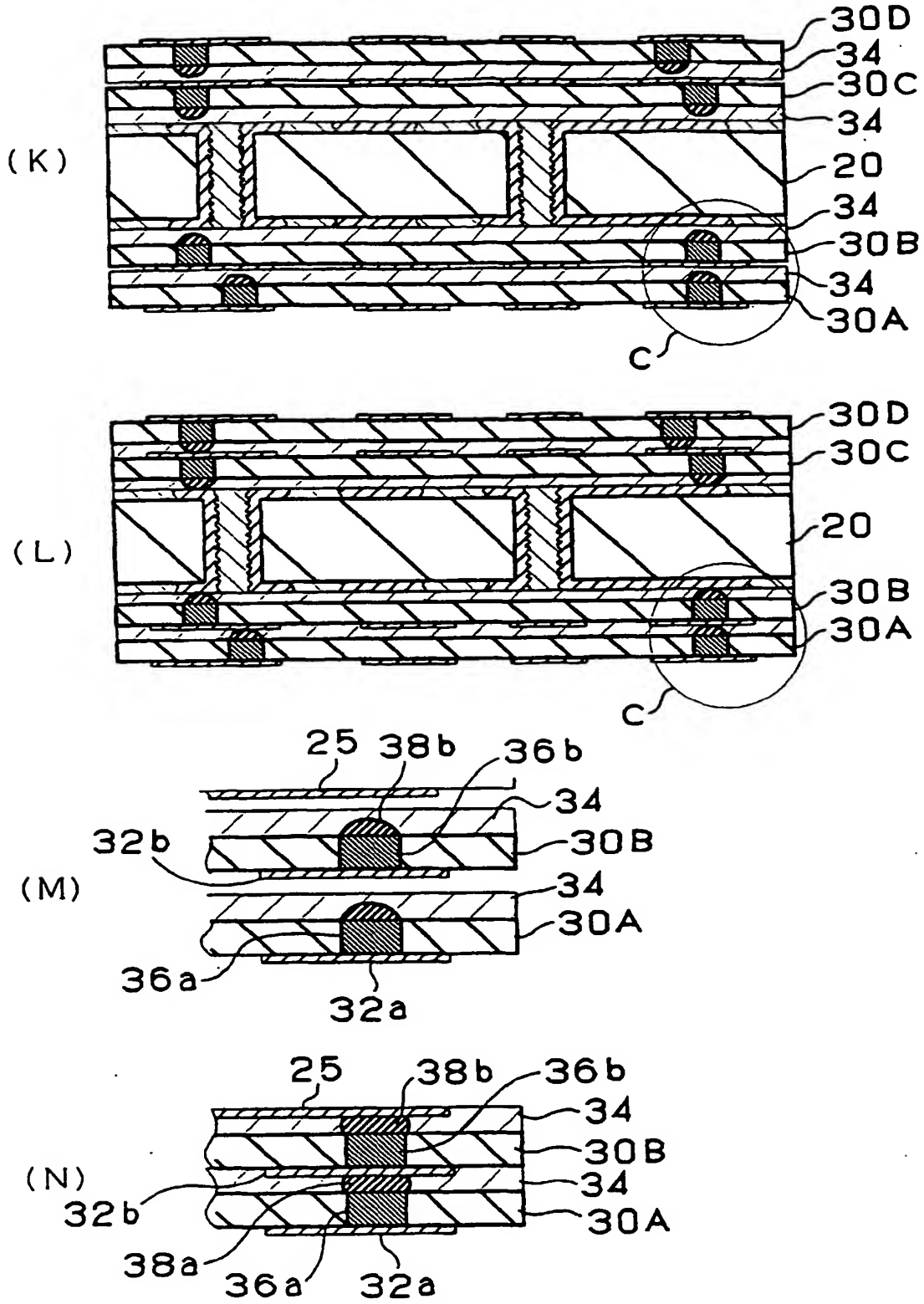

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Fig.6

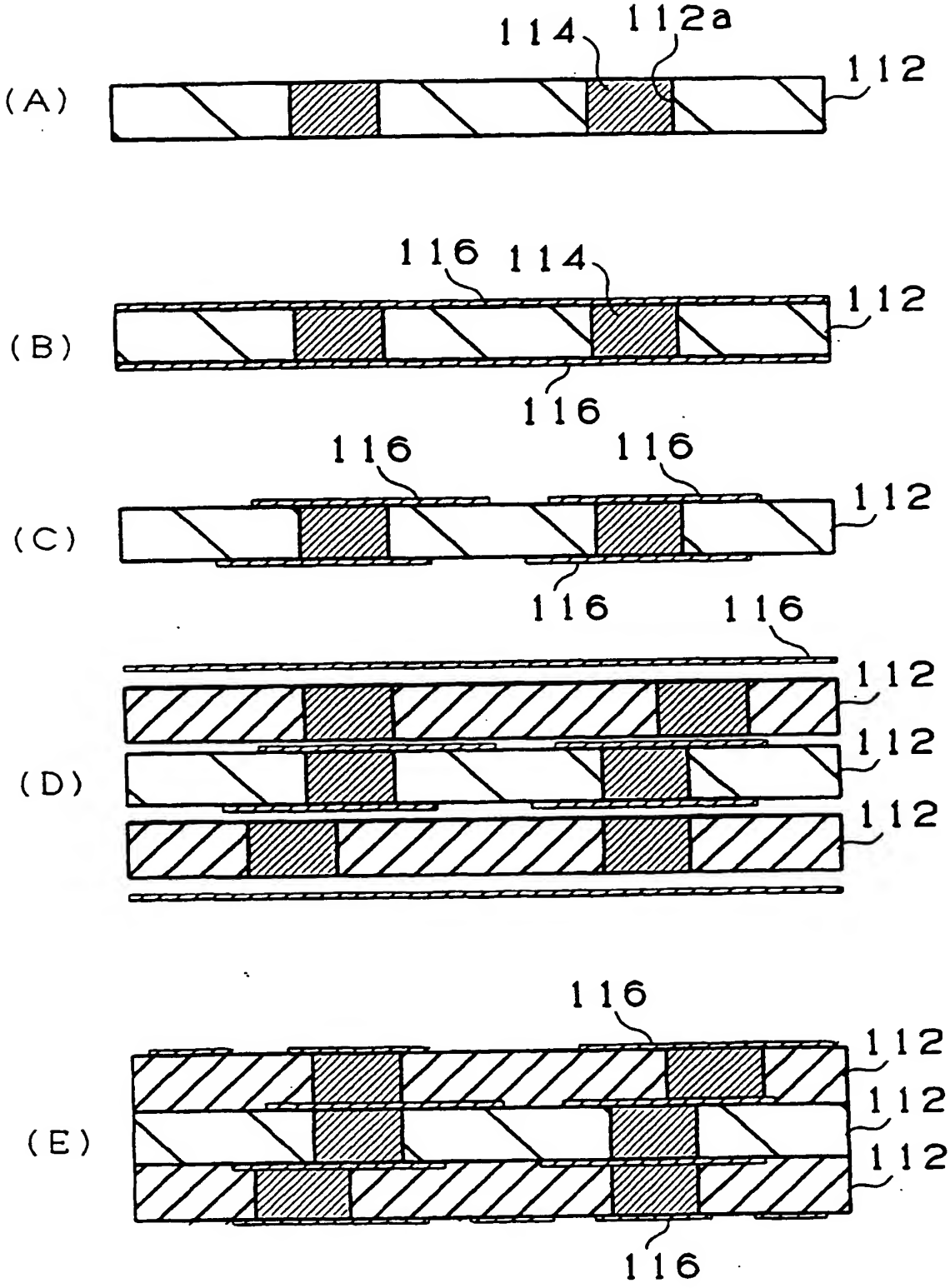

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Fig. 7

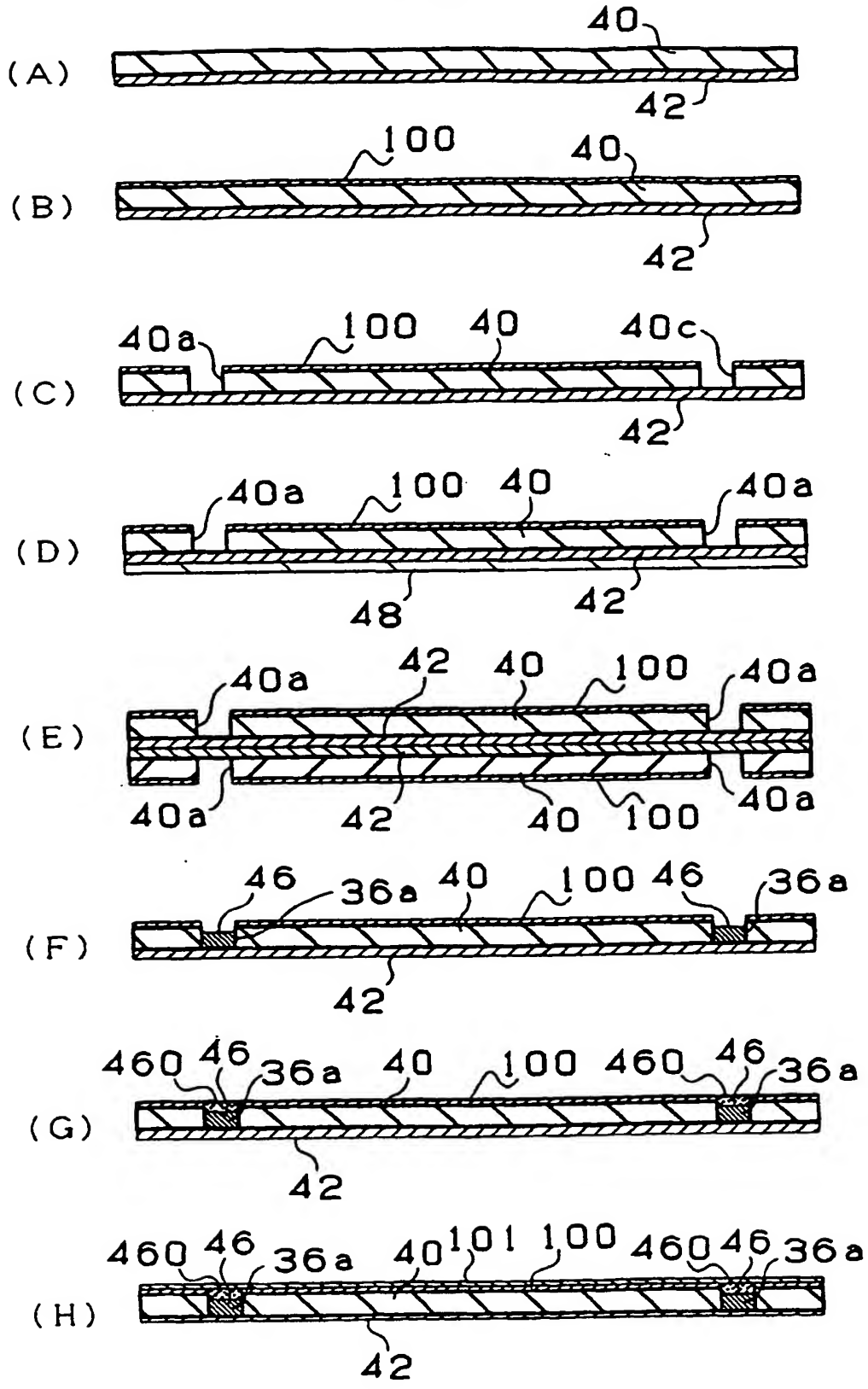

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Fig.8

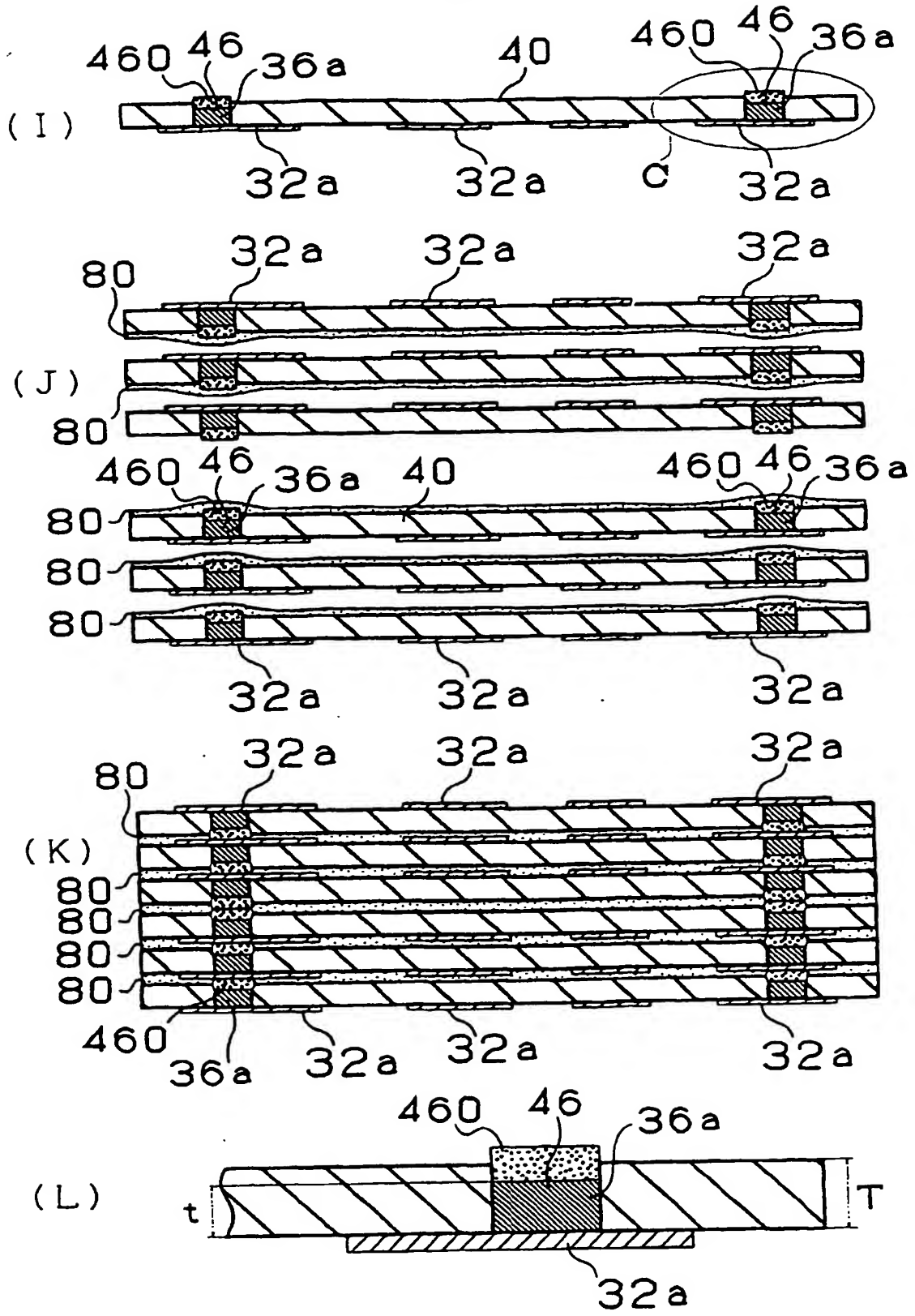

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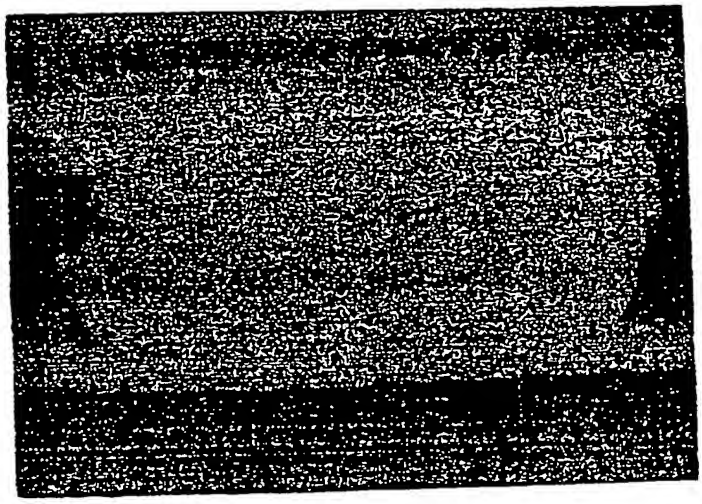
Fig. 9



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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP98/02497

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl⁶ H05K3/46

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl⁶ H05K3/46, H05K3/00, H05K3/40, H05K1/11

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1926-1996 Toroku Jitsuyo Shinan Koho 1994-1998
Kokai Jitsuyo Shinan Koho 1971-1998 Jitsuyo Shinan Toroku Koho 1996-1998

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP, 6-326438, A (Nitto Denko Corp.), November 25, 1994 (25. 11. 94), Par. Nos. [0029], [0030] (Family: none)	1-12
E, X	JP, 10-117067, A (Shinko Electric Industries Co., Ltd.), May 6, 1998 (06. 05. 98), Par. Nos. [0009] to [0014] (Family: none)	1-12
A	JP, 4-162589, A (NEC Corp.), June 8, 1992 (08. 06. 92) (Family: none)	1-12

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
August 18, 1998 (18. 08. 98)	August 25, 1998 (25. 08. 98)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)

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